AMENDMENTS TO THE CLAIMS

1. (Previously presented). A parallel joining technology method for making a multi-layer electronic structure, the method comprising:

providing a plurality of sub-composites, wherein each said sub-composite is formed by the steps of

providing a layer of dielectric material having a first surface and a second surface, wherein said first surface is selected from the group consisting of a top surface and a bottom surface,

providing a layer of electrically conducting material on said first surface;

forming at least one blind via comprising a passage from said second surface through said dielectric layer to expose said layer of electrically conducting material facing said dielectric layer;

depositing electrically conducting metallurgical material in at least one of said blind vias wherein said electrically conducting layer is in electrical contact with said electrically conductive metallurgical material in said at least one blind via;

removing portions of the layer of electrically conducting material to define a pattern of circuitry;

stacking a plurality of said sub-composites;

aligning said plurality of sub-composites;

joining said plurality of sub-composites such that the electrically conducting metallurgical material in at least one of said blind vias makes electrical contact by forming a metallurgical bond to the conductive pattern on an adjacent sub-composite; and

filling spaces between adjacent sub-composites with electrically insulating material.

2. (Previously presented). The method according to claim 79, wherein the dielectric material is selected from the group consisting of free standing organic film, fiber reinforced resin sheet, particulate filled fluoropolymer sheet, or resin filled expanded fluoropolymer sheet.

3. (Previously presented). The method according to claim 2, wherein the free standing organic film is polyimide film.

4. (Previously presented). The method according to claim 2, wherein the free standing organic film is a liquid crystal polymer film.

5. (Previously presented). The method according to claim 2, wherein the fiber reinforced resin sheet includes at least one of glass, aramid, and liquid crystal polymer fibers and the fibers are woven or non-woven.

6. (Previously presented). The method according to claim 1, wherein a layer of electrically conducting material is provided on both the top surface and the bottom surface of the layer of dielectric material, the method further comprising removing a layer of conductive material on one of the top and bottom surface.

7. (Previously presented). The method according to claim 1, wherein the layer of electrically conducting material is patternable is solderable or can have a solderable surface layer applied.

8. (Previously presented). The method according to claim 1, wherein the layer of electrically conducting material comprises at least one metal.

9. (Previously presented). The method according to claim 1, wherein the layer of electrically conducting material comprises copper.

10. (Previously presented). The method according to claim 1, wherein the layer of electrically conducting material is provided by a method selected from the group consisting of lamination, physical vapor deposition, plating, and chemical vapor deposition.

11. (Previously presented). The method according to claim 10, wherein the physical vapor deposition comprises vacuum evaporation or sputtering.

12. (Previously presented). The method according to claim 10, wherein the plating comprises electroplating or electroless plating.

13. (Previously presented). The method according to claim 1, wherein the layer of dielectric material is provided by applying dielectric material to the layer of electrically conducting material.

14. (Previously presented). The method according to claim 13, wherein the electrically conducting material comprises copper.

15. (Previously presented). The method according to claim 13, wherein the dielectric material is applied to an electrically conductive foil by a method selected from the group consisting of screening, slot coating, curtain coating, doctor blading, roll coating, rod coating, dip coating, and spraying.

16. (Previously presented). The method according to claim 1, further comprising:

applying a layer of a protective material on the layer of electrically conducting material.

17. (Previously presented). The method according to claim 1, wherein the at least one passage through the dielectric layer is formed by laser drilling or plasma etching.

18. (Previously presented). The method according to claim 1, wherein the electrically conducting metallurgical material deposited in at least one of the at least one passage through the dielectric layer does not extend beyond an opening of the at least one passage.

19. (Previously presented). The method according to claim 1, wherein the electrically conducting metallurgical material deposited in at least one of the at least one passage through the dielectric layer ~~does~~ at least partially extends beyond an opening of the at least one passage.

20. (Previously presented). The method according to claim 79, wherein the electrically conducting metallurgical material is deposited in at least one of the at least one passage through the dielectric layer by plating or introducing electrically conducting paste into the at least one passage.

21. (Previously presented). The method according to claim 20, wherein the electrically conducting metallurgical material is deposited in at least one of the at least one passage through the dielectric layer by plating and the plating is electroplating or electroless plating.

22. (Previously presented). The method according to claim 79, wherein the electrically conducting metallurgical material is deposited in at least one of the at least one passage through the dielectric layer by introducing electrically conducting paste into the at least one passage, wherein the introduction of the electrically conducting paste comprises forcing the conducting paste into the at least one passage and curing the conducting paste.

23. (Previously presented). The method according to claim 22, wherein forcing the conducting paste into the at least one passage comprises squeegeeing the conducting paste.

24. (Previously presented). The method according to claim 1, further comprising: providing a cap on the electrically conducting metallurgical material in the at least one passage.

25. (Previously presented). The method according to claim 24, wherein the cap comprises tin.

26. (Previously presented). The method according to claim 24, wherein the cap comprises a tin-containing alloy.

27. (Previously presented). The method according to claim 24, wherein the cap has a thickness of about 0.0001 inch to about 0.0004 inch.

28. (Previously presented). The method according to claim 24, wherein the cap is provided by plating an electrically conducting material on the electrically conducting material in the at least one passage.

29. (Previously presented). The method according to claim 28, wherein the plating is electroplating or electroless plating.

30. (Previously presented).The method according to claim 28, wherein the plating is maskless and self-aligning.

31. (Previously presented). The method according to claim 1, further comprising:

applying a protecting coating over the layer of electrically conducting material on the dielectric layer, wherein the protecting layer is removed prior to removing portions of the layer of electrically conducting material to define a pattern of circuitry.

32. (Previously presented). The method according to claim 1, wherein removing portions of the layer of electrically conducting material to define a pattern of circuitry comprises depositing a layer of photoresist on the layer of electrically conducting material, exposing the photoresist, developing the photoresist to form a mask for selectively removing portions of the layer of electrically conducting material, and removing remaining portions of the photoresist.

33. (Previously presented). The method according to claim 1, further comprising:

treating the layer of dielectric material and the pattern of circuitry with an immersion tin plating solution.

34. (Previously presented). The method according to claim 1, further comprising:

treating the layer of dielectric material and the pattern of circuitry in a fluorine-containing plasma.

35. (Previously presented). The method according to claim 1, wherein the structures are aligned with at least one of aligning pins and aligning marks.

36. (Previously presented). The method according to claim 1, wherein the structures are stacked one-by-one and each time another structure is added to the stack it is soldered to a structure in the stack.

37. (Previously presented). The method according to claim 1, wherein forming a metalurgical bond comprises heating the structures to a temperature above a melting point of at least one of the constituent of, or the cap deposited on, the electrically conducting metallurgical material deposited in the at least one passage in the dielectric layer.

38. (Previously presented). The method according to claim 37, wherein joining the structures further comprises applying pressure to the stack from above and below.

39. (Previously presented). The method according to claim 37, wherein the joining is carried out in an atmosphere that is inert under the conditions that the joining is carried out under.

40. (Previously presented). The method according to claim 39, wherein the joining is carried out in a nitrogen atmosphere.

41. (Previously presented). The method according to claim 37, wherein the joining is carried out under a vacuum.

42. (Previously presented). The method according to claim 1, wherein the spaces between the structures are filled with a low viscosity, thermosetting resin.

43. (Previously presented). The method according to claim 42, wherein filling the spaces comprises arranging a gas impermeable flexible covering about the plurality of structures, sealing a periphery of the plurality of structures in the vicinity a top and a bottom surface of the plurality of structures, and introducing the resin into the covering.

44. (Previously presented). The method according to claim 43, wherein after introduction the resin is cured.

45. (Previously presented). The method according to claim 16, wherein the protective material is photoresist.

46. (Previously presented). A parallel joining technology multi-layer electronic structure, comprising:

at least two substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface or the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conductive metallurgical material, the at least two substructures being stacked on each other such that one of the electrically conducting material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by means of a metallurgical bond to one of the electrically conductive metallurgical material filling the at least one passage and the circuitry pattern on another substructure; and

electrically insulating material substantially filling a space between facing substructures except between a joined filled passage and circuitry pattern.

47. (Previously presented). The structure according to claim 46, wherein the dielectric material is selected from the group consisting of free standing organic film, fiber reinforced resin sheet, or particulate filled fluoropolymer sheet, or resin filled expanded fluoropolymer sheet.

48. (Previously presented). The structure according to claim 47, wherein the free standing organic film is polyimide film.

49. (Previously presented). The structure according to claim 47, wherein the free standing organic film is a liquid crystal polymer film.

50. (Previously presented). The structure according to claim 47, wherein the fiber reinforced resin sheet includes at least one of glass aramid, and liquid crystal polymer fibers and the fibers are woven or non-woven.

51. (Previously presented). The structure according to claim 46, wherein the layer of electrically conducting material comprises at least one metal.

52. (Previously presented). The structure according to claim 46, wherein the layer of electrically conducting material comprises copper.

53. (Previously presented). The structure according to claim 80, wherein the electrically conducting metallurgical material deposited in the at least one passage through the dielectric layer comprises at least one metal, alloy, or electrically conducting paste.

54. (Previously presented). The structure according to claim 80, further comprising:

a cap on the electrically conducting metallurgical material in the at least one passage.

55. (Previously presented). The structure according to claim 54, wherein the cap comprises tin.

56. (Previously presented). The structure according to claim 54, wherein the cap comprises a tin-containing alloy.

57. (Previously presented). The structure according to claim 54, wherein the cap has a thickness of about 0.0001 inch to about 0.0004 inch.

58. (Previously presented). The structure according to claim 46, further comprising:

a layer of tin oxide on the pattern of circuitry.

59. (Previously presented). The structure according to claim 46, wherein the layer of dielectric material and the pattern of circuitry have been treated in a fluorine-containing plasma prior to stacking and joining the substructures.

60. (Previously presented). The structure according to claim 46, further comprising:

an aligning structure for aligning the substructures.

61. (Previously presented). The structure according to claim 60, wherein the aligning structure comprises at least one aligning passage for receiving an aligning pin.

62. (Previously presented). The structure according to claim 60, wherein the aligning structure comprises at least one aligning mark on each substructure.

63. (Previously presented). The structure according to claim 46, wherein the substructures are soldered together.

64. (Previously presented). The structure according to claim 46, wherein the spaces between the structures are filled with a low viscosity, thermosetting resin.

65. (Previously presented). The structure according to claim 64, wherein the resin is cured.

66. (Previously presented). A parallel joining technology electronic package, comprising:

a multi-layer structure comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting metallurgical material, the at least two substructures being stacked on each other such that one of the electrically conducing metallurgical material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined to one of the electrically conducting metallurgical material filling the at least one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and

a semiconductor chip attached to the multi-layer structure.

67. (Previously presented) A parallel joining technology electronic package, comprising:

a printed wiring board comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting metallurgical material, the at least two substructures being stacked on each other such that one of the electrically conducting metallurgical material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined to one of the electrically conducting metallurgical material filling the at lease one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and

a plurality of electronic components attached to the printed wiring board.

68. (Previously presented). A parallel joining technology method for making a multi-layer electronic interconnect structure, the method comprising:

providing a layer of dielectric material bonded to a layer of electrically conductive material, the layer of dielectric material having substantially uniform thickness;

forming at least one passage through the layer of dielectric material to expose a portion of the layer of electrically conductive material;

depositing electrically conducting metallurgical material in at least one of the at least one passage through the layer of dielectric material, such that the electrically conducting metallurgical material in the at least one passage is in electrical contact with the layer of

electrically conducting material bonded to the layer of dielectric material and extends beyond a surface of the layer of dielectric material;

removing portions of the layer of electrically conducting material to define a pattern of circuit conductors, such that at least one of the circuit conductors remains electrically connected to the electrically conductive metallurgical material deposited in that at least one of the at least one passage through the layer of dielectric material;

stacking and aligning a plurality of structures comprising the layer of dielectric material with circuit conductors disposed thereon and conductively filled passages therethrough such that one of the following conditions exists:

a) at least one conductively filled passage in a structure contacts at least one circuit conductor on the conductive layer of an adjacent structure,

b) at least one circuit conductor on the conductive layer of a structure contacts at least one conductively filled passage in an adjacent structure, or

c) at least one conductively filled passage in a structure contacts at least one conductively fined passage in an adjacent structure;

electrically and mechanically joining the electrically conductive metallurgical material filling one of the at least one passage that is aligned with an electrically conductive feature on an adjacent structure to the adjacent structure conductive features; and

filling spaces between the adjacent structures with an electrically insulating material.

69. (Previously presented).The method according to claim 68, wherein the electrically insulating material used to fill spaces between the adjacent structures comprises a liquid which is transformed into a solid subsequent to filling the spaces.

70. (Previously presented).The method according to claim 69, wherein the transformable insulating material is an organic resin.

71. (Previously presented). The method according to claim 70, wherein the organic resin includes at least one member selected from the group consisting of epoxy, acrylic, cyanate ester, urethane, polyester, bismaleimide triazine, silicone, and mixtures or copolymers thereof.

72. (Previously presented). The method according to claim 70, wherein the transformable electrically insulating material comprises at least one inorganic particulate filler in an amount up to about 60 percent by volume.

73. (Previously presented). The method according to claim 70, wherein the transformable electrically insulating material is converted to a solid by at least one means selected from the group consisting of chemical polymerization and cross linking reactions.

74. (Previously presented). The method according to claim 68, wherein filling spaces between adjacent structures comprises introducing a liquid electrically insulating material into the spaces and allowing capillary forces to transport the liquid from a point of introduction throughout the spaces.

75. (Previously presented). The method according to claim 74, wherein the liquid electrically insulating material is introduced at least one point around peripheries of the layers of dielectric material.

76. (Previously presented). The method according to claim 74, wherein the liquid electrically insulating material is introduced at a pressure greater than atmospheric pressure in order to provide a larger driving force for material transport than provided by capillary forces alone.

77. (Previously presented). The method according to claim 74, wherein a vacuum is created and maintained in spaces between the adjacent structures during a time when the liquid electrically insulating material is being introduced.

78. (Previously presented). The method according to claim 77, further comprising:

arranging a gas impermeable flexible covering about the plurality of structures;

sealing the flexible covering to the plurality of structures about top and bottom peripheries of the structures;

evacuating the atmosphere from within the flexible covering;

introducing a liquid electrically insulating material into the evacuated covering in the vicinity of at least one edge of the plurality of structures;

allowing the liquid electrically insulating material to fill the spaces between structures;

transforming the liquid electrically insulating material into a solid; and

removing the gas impermeable covering.

79. (Currently amended). The method of claim 1 wherein said electrically conducting metallurgical material comprises a material selected from the group consisting of a plated metal, a plated alloy, a conductive paste having metal particles, at least a portion of which are fusible, present in a volume fraction above a percolation threshold, a conductive paste having fusible metal particles, and a conductive paste having metal particles coated with a fusible metal coating.

80. (Currently amended). The structure of claim 46 wherein said electrically conducting metallurgical material comprises a material selected from the group consisting of a plated metal, a plated alloy, a conductive paste having metal particles, at least a portion of which are fusible, present in a volume fraction above a percolation threshold, a conductive paste having fusible metal particles, and a conductive paste having metal particles coated with a fusible metal coating.